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84300 Dual-In-Line Delay Module, TTL Compatible 14 Pin
5 Equally Spaced Taps with integrated decoupling capacitor

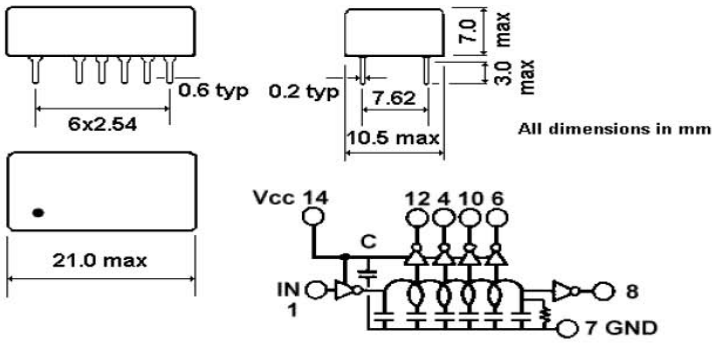
Basic Specification

```
Delay Range -------------------- 25nS to 500 nS ± 5% or ±2nS, whichever is greater
Tap to Tap Tolerances ---------- ±10% of delay between taps or ±1nS, whichever is greater
Rise Time ---------------------- 4nS Maximum
Supply Voltage (Vcc) ----------- 5.0V ±5%
Supply Current ----------------- 60mA (Typical) with 10 TTL loads
Logic 0 Input Current ---------- 2mA Maximum
Logic 1 Input Current ---------- 50uA Maximum
Logic 0 Voltage Out ------------ 0.4V Maximum
Logic 1 Voltage Out ------------ 2.4V Minimum
Fan out Capabilities ----------- 10 TTL loads/tap Max. or 20 TTL loads/Delay Network Max
Operating Temperatures --------- 0 °C to +70 °C
Humidity ----------------------- Conforms with BS.2011, Class H2
Vibration---------------------- Conforms with MIL.STD.202, Method 204
Solderability ------------------ Connecting pins solderable to BS.2011:2T
```

Input Test Conditions

```
Vcc ---------------------------- 5.0V
Supply Current ----------------- 60mA
Pulse Voltage ------------------ 3.2V
Pulse Width -------------------- 50% of Total Delay Minimum
Rise Time ---------------------- 2nS
Temperature -------------------- 25°C ±20%
Loadings ----------------------- 2 TTL loads/tap (10 total)
```

Tap to Tap Delay Time	Total Delay Time	Ordering Detail Number
5nS	25nS	84301
6nS	30nS	84302
7nS	35nS	84303
8nS	40nS	84304
9nS	45nS	84305
10nS	50nS	84306
15nS	75nS	84307
20nS	100nS	84308
30nS	150nS	84309
40nS	200nS	84310
50nS	250nS	84311
60nS	300nS	84312
70nS	350nS	84313
80nS	400nS	84314
90nS	450nS	84315
100nS	500nS	84316



All Above Delay Networks incorporate a 0.01μf Decoupling Capacitor 'C' between Vcc and GND(7)