

LEXOR

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84360 Dual-In-Line Delay Module, TTL Compatible 14 Pin 5 Equally Spaced Taps with integrated decoupling capacitor. Incorporating 54SO4 I.C. to 883B Standard

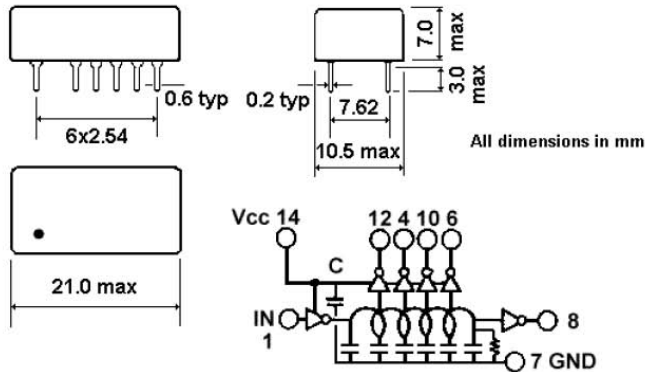
Basic Specification

Delay Range ----- 25nS to 500 nS \pm 5% or \pm 2nS, whichever is greater
 Tap to Tap Tolerances ----- \pm 10% of delay between taps or \pm 1nS, whichever is greater
 Rise Time ----- 4nS Maximum
 Supply Voltage (Vcc) ----- 5.0V \pm 5%
 Supply Current ----- 60mA (Typical) with 10 TTL loads
 Logic 0 Input Current ----- 2mA Maximum
 Logic 1 Input Current ----- 50uA Maximum
 Logic 0 Voltage Out ----- 0.4V Maximum
 Logic 1 Voltage Out ----- 2.4V Minimum
 Fan out Capabilities ----- 10 TTL loads/tap Max. or 20 TTL loads/Delay Network Max
 Operating Temperatures ----- 55 °C to +125 °C
 Humidity ----- Conforms with BS.2011, Class H2
 Vibration----- Conforms with MIL.STD.202, Method 204
 Solderability ----- Connecting pins solderable to BS.2011:2T
 Encapsulation ----- Flame Retardant Epoxy Resin

Input Test Conditions

Vcc ----- 5.0V
 Supply Current ----- 60mA
 Pulse Voltage ----- 3.2V
 Pulse Width ----- 50% of Total Delay Minimum
 Rise Time ----- 2nS
 Temperature ----- 25°C \pm 20%
 Loadings ----- 2 TTL loads/tap (10 total)

Tap to Tap Delay Time	Total Delay Time	Ordering Detail Number
5nS	25nS	84361
6nS	30nS	84362
7nS	35nS	84363
8nS	40nS	84364
9nS	45nS	84365
10nS	50nS	84366
15nS	75nS	84367
20nS	100nS	84368
30nS	150nS	84369
40nS	200nS	84370
50nS	250nS	84371
60nS	300nS	84372
70nS	350nS	84373
80nS	400nS	84374
90nS	450nS	84375
100nS	500nS	84376



All Above Delay Networks incorporate a 0.01 μ f Decoupling Capacitor 'C' between Vcc and GND(7)