LEXOR

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84540 Dual-In-Line Delay Module, TTL Compatible
14 Pin-Triple Logic Taps with integrated decoupling capacitor.
Incorporating 54SO4 I.C. to 883B Standard

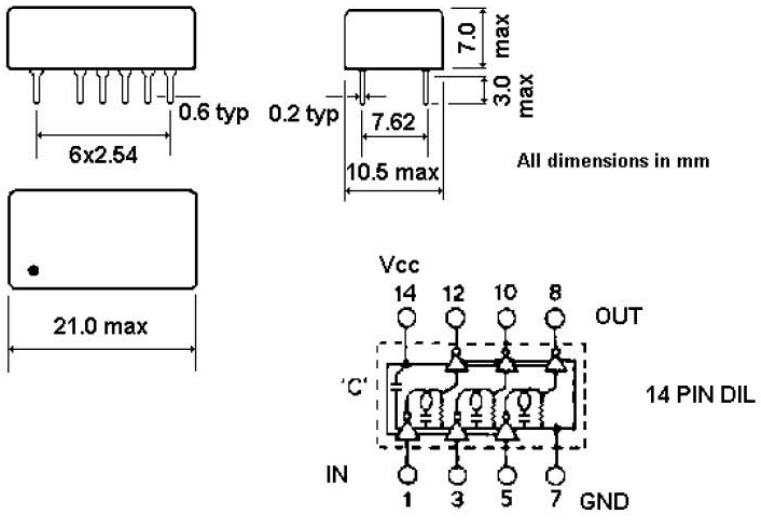
Basic Specification

Delay Range ---------- 25nS to 500 nS ± 5% or ±2nS, whichever is greater Tap to Tap
Tolerances ---------- ±10% of delay between taps or ±1nS, whichever is greater
Rise Time ---------- 4nS Maximum
Supply Voltage (Vcc) ---------- 5.0V ±5%
Supply Current ---------- 60mA (Typical) with 10 TTL loads
Logic 0 Input Current ---------- 2mA Maximum
Logic 1 Input Current ---------- 50uA Maximum
Logic 0 Voltage Out ---------- 0.4V Maximum
Logic 1 Voltage Out ---------- 2.4V Minimum
Fan out Capabilities ---------- 10 TTL loads/tap Max. or 20 TTL loads/Delay Network Max
Operating Temperatures ----------25 °C to +125 °C
Humidity ---------- Conforms with BS.2011, Class H2
Vibration---------- Conforms with MIL.STD.202, Method 204
Solderability ---------- Connecting pins solderable to BS.2011:2T
Encapsulation ---------- Flame Retardant Epoxy Resin

Input Test Conditions

Vcc ---------- 5.0V
Supply Current ---------- 60mA
Pulse Voltage ---------- 3.2V
Pulse Width ---------- 100% of Total Delay Minimum
Rise Time ---------- 2nS
Temperature ---------- 25°C ±20%
Loadings ---------- 2 TTL loads/section (6 total)

Total Delay Time	Ordering Detail Number
3 x 25nS	84501
3 x 30nS	84502
3 x 35nS	84503
3 x 40nS	84504
3 x 45nS	84505
3 x 50nS	84506
3 x 75nS	84507
3 x 100nS	84508
3 x 150nS	84509
3 x 200nS	84510
3 x 250nS	84511
3 x 300nS	84512
3 x 350nS	84513
3 x 400nS	84514
3 x 450nS	84515
3 x 500nS	84516



All Above Delay Networks incorporate a 0.01µf Decoupling Capacitor 'C' between Vcc and GND(7)