

# LEXOR

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## 86360 Dual-In-Line Delay Module, TTL Compatible 14 Pin 5 Equally Spaced Taps with integrated decoupling capacitor Low Power Consumption/High Speed, incorporating 54FO4 I.C. to 883B Standard

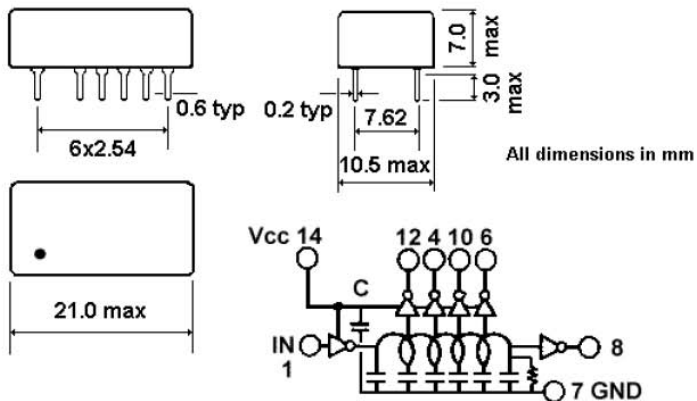
### Basic Specification

Delay Range ----- 25nS to 500 nS  $\pm$  5% or  $\pm$ 2nS, whichever is greater  
 Tap to Tap Tolerances -----  $\pm$ 10% of delay between taps or  $\pm$ 1nS, whichever is greater  
 Rise Time ----- 3nS Maximum  
 Supply Voltage (Vcc) ----- 5.0V  $\pm$ 5%  
 Supply Current ----- 10mA (Typical) with 10 TTL loads  
 Logic 0 Input Current ----- 1mA Maximum  
 Logic 1 Input Current ----- 50uA Maximum  
 Logic 0 Voltage Out ----- 0.4V Maximum  
 Logic 1 Voltage Out ----- 2.4V Minimum  
 Fan out Capabilities ----- 10 TTL loads/tap Max. or 20 TTL loads/Delay Network Max  
 Operating Temperatures ----- 25 °C to +125 °C  
 Humidity ----- Conforms with BS.2011, Class H2  
 Vibration----- Conforms with MIL.STD.202, Method 204  
 Solderability ----- Connecting pins solderable to BS.2011:2T  
 Encapsulation ----- Flame Retardant Epoxy Resin

### Input Test Conditions

Vcc ----- 5.0V  
 Supply Current ----- 10mA  
 Pulse Voltage ----- 3.2V  
 Pulse Width ----- 50% of Total Delay Minimum  
 Rise Time ----- 2nS  
 Temperature ----- 25°C  $\pm$ 20%  
 Loadings ----- Taps 1-4, 2 TTL loads. Output 5 TTL Loads

Tap to Tap Delay Time	Total Delay Time	Ordering Detail Number
3	15nS	86379
4	20nS	86378
5	25nS	86361
6	30nS	86362
7	35nS	86363
8	40nS	86364
9	45nS	86365
10	50nS	86366
15	75nS	86367
20	100nS	86368
25	125nS	86377
30	150nS	86369
40	200nS	86370
50	250nS	86371
60	300nS	86372
70	350nS	86373
80	400nS	86374
90	450nS	86375
100	500nS	86376



All Above Delay Networks incorporate a 0.01 $\mu$ f Decoupling Capacitor 'C' between Vcc and GND(7)