

LEXOR

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86600 Dual-In-Line Delay Module, TTL Compatible 14 Pin Triple Logic with integrated decoupling capacitor.

Low Power Consumption/High Speed, incorporating 54F04 I.C. to 883B Standard

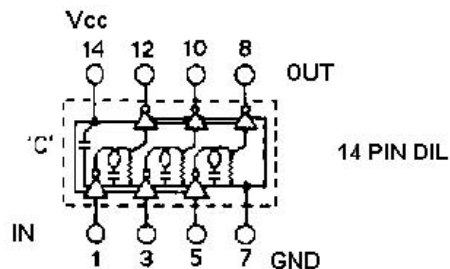
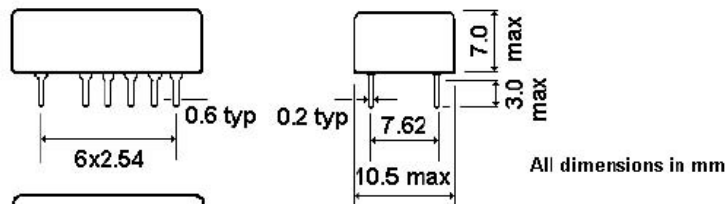
Basic Specification

Delay Range ----- 25nS to 500 nS \pm 5% or \pm 2nS, whichever is greater
 Tap to Tap Tolerances ----- \pm 10% of delay between taps or \pm 1nS, whichever is greater
 Rise Time ----- 3nS Maximum
 Supply Voltage (Vcc) ----- 5.0V \pm 5%
 Supply Current ----- 10mA (Typical) with 10 TTL loads
 Logic 0 Input Current ----- 1mA Maximum
 Logic 1 Input Current ----- 50uA Maximum
 Logic 0 Voltage Out ----- 0.4V Maximum
 Logic 1 Voltage Out ----- 2.4V Minimum
 Fan out Capabilities ----- 10 TTL loads/tap Max. or 20 TTL loads/Delay Network Max
 Operating Temperatures ----- 55 °C to +125 °C
 Humidity ----- Conforms with BS.2011, Class H2
 Vibration----- Conforms with MIL.STD.202, Method 204
 Solderability ----- Connecting pins solderable to BS.2011:2T
 Encapsulation ----- Flame Retardant Epoxy Resin

Input Test Conditions

Vcc ----- 5.0V
 Supply Current ----- 10mA
 Pulse Voltage ----- 3.2V
 Pulse Width ----- 100% of Total Delay Minimum
 Rise Time ----- 2nS
 Temperature ----- 25°C \pm 20%
 Loadings ----- 2 TTL loads/section (6 total)

Total Delay Time	Ordering Detail Number
3 x 25nS	86601
3 x 30nS	86602
3 x 35nS	86603
3 x 40nS	86604
3 x 45nS	86605
3 x 50nS	86606
3 x 75nS	86607
3 x 100nS	86608
3 x 150nS	86609
3 x 200nS	86610
3 x 250nS	86611
3 x 300nS	86612
3 x 350nS	86613
3 x 400nS	86614
3 x 450nS	86615
3 x 500nS	86616



All Above Delay Networks incorporate a 0.01 μ f Decoupling Capacitor 'C' between Vcc and GND(7)