

# LEXOR

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## 87360 Dual-In-Line Delay Module, TTL Compatible 14 Pin 5 Equally Spaced Taps with integrated decoupling capacitor Minimal Power Consumption, incorporating 54HCT04 I.C. to 883B Standard

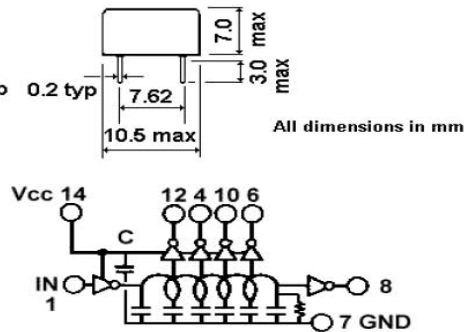
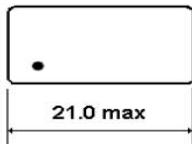
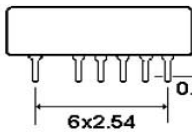
### Basic Specification

Delay Range ----- 25nS to 500 nS  $\pm$  5% or  $\pm$ 2nS, whichever is greater  
 Tap to Tap Tolerances -----  $\pm$ 10% of delay between taps or  $\pm$ 1nS, whichever is greater Rise  
 Time ----- 3nS Maximum  
 Supply Voltage (Vcc) ----- 5.0V  $\pm$ 5%  
 Supply Current ----- 1uA (Quiescent)  
 Logic 0 Input Current ----- 1uA Maximum  
 Logic 1 Input Current ----- 1uA Maximum  
 Logic 0 Voltage Out ----- 0.4V Maximum  
 Logic 1 Voltage Out ----- 2.4V Minimum  
 Fan out Capabilities ----- 10 TTL loads/tap Max. or 20 TTL loads/Delay Network Max  
 Operating Temperatures ----- -25 °C to +125 °C  
 Humidity ----- Conforms with BS.2011, Class H2  
 Vibration----- Conforms with MIL.STD.202, Method 204  
 Solderability ----- Connecting pins solderable to BS.2011:2T  
 Encapsulation ----- Flame Retardant Epoxy Resin

### Input Test Conditions

Vcc ----- 5.0V  
 Supply Current ----- 8mA (50% M:S)  
 Pulse Voltage ----- 3.2V  
 Pulse Width ----- 50% of Total Delay Minimum  
 Rise Time ----- 2nS  
 Temperature ----- 25°C  $\pm$ 20%  
 Loadings ----- Taps 1-4, 2 TTL loads. Output 5 TTL Loads

Tap to Tap Delay Time	Total Delay Time	Ordering Detail Number
10nS	50nS	87366
15nS	75nS	87367
20nS	100nS	87368
25nS	125nS	87377
30nS	150nS	87369
40nS	200nS	87370
50nS	250nS	87371
60nS	300nS	87372
70nS	350nS	87373
80nS	400nS	87374
90nS	450nS	87375
100nS	500nS	87376



All dimensions in mm

All Above Delay Networks incorporate a 0.01 $\mu$ F Decoupling Capacitor 'C' between Vcc and GND(7)