

# LEXOR

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## 87600 Dual-In-Line Delay Module, HCTMOS, TTL Compatible 14 Pin

Triple Logic, with integrated decoupling capacitor.

Minimal Power Consumption, incorporating 54HCT04 I.C. to 883B Standard

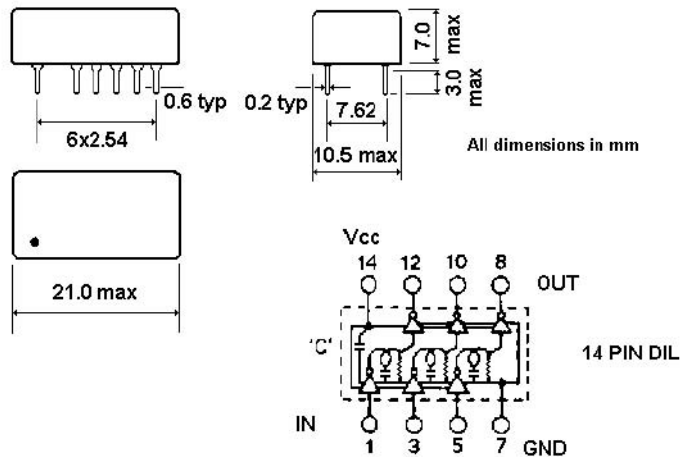
### Basic Specification

Delay Range ----- 25nS to 500 nS  $\pm$  5% or  $\pm$ 2nS, whichever is greater  
 Tap to Tap Tolerances -----  $\pm$ 10% of delay between taps or  $\pm$ 1nS, whichever is greater  
 Rise Time ----- 7nS Maximum  
 Supply Voltage (Vcc) ----- 5.0V  $\pm$ 5%  
 Supply Current ----- 1uA (Quiescent)  
 Logic 0 Input Current ----- 1uA Maximum  
 Logic 1 Input Current ----- 1uA Maximum  
 Logic 0 Voltage Out ----- 0.4V Maximum  
 Logic 1 Voltage Out ----- 2.4V Minimum  
 Fan out Capabilities ----- 10 TTL loads/tap Max. or 20 TTL loads/Delay Network Max  
 Operating Temperatures ----- -25 °C to +125 °C  
 Humidity ----- Conforms with BS.2011, Class H2  
 Vibration----- Conforms with MIL.STD.202, Method 204  
 Solderability ----- Connecting pins solderable to BS.2011:2T  
 Encapsulation ----- Flame Retardant Epoxy Resin

### Input Test Conditions

Vcc ----- 5.0V  
 Supply Current ----- 8mA (50% M:S)  
 Pulse Voltage ----- 3.2V  
 Pulse Width ----- 100% of Total Delay Minimum  
 Rise Time ----- 2nS  
 Temperature ----- 25°C  $\pm$ 20%  
 Loadings ----- 2 TTL loads/section (6 total)

Total Delay Time	Ordering Detail Number
3 x 25nS	87601
3 x 30nS	87602
3 x 35nS	87603
3 x 40nS	87604
3 x 45nS	87605
3 x 50nS	87606
3 x 75nS	87607
3 x 100nS	87608
3 x 150nS	87609
3 x 200nS	87610
3 x 250nS	87611
3 x 300nS	87612
3 x 350nS	87613
3 x 400nS	87614
3 x 450nS	87615
3 x 500nS	87616



All Above Delay Networks incorporate a 0.01 $\mu$ F Decoupling Capacitor 'C' between Vcc and GND(7)